Universidad de Navarra

Digital Systems (Ing.Gr.)
Guía docente 2026-27

PRESENTATION

Brief description:

The main objective of the course is to set the basis of digital electronics for electronics and telecommunication engineers. The course starts with advanced concepts of combinational devices and then focuses on sequential circuits and their design. Finally, an introduction to A/D and D/A converters is also taught.

Titulación (Módulo/Materia):

- Ingeniería en Electrónica Industrial (Bloque Especializado de Electrónica Industrial /SistemasDigitales y Control)

Detalles:

- **ECTS**: 4 ECTS
- **Curso, semestre**: 3.º curso, 1.º semestre
- **Carácter**: Obligatorio
- **Idioma**: Inglés

Profesores de la asignatura:

- García Mandayo, Gemma / Catedrática
- García Muñoz, Francisco Javier / Colaborador docente
- Solar Ruiz, Héctor / Profesor titular
- Sánchez Basterrechea, Manuel / Colaborador docente

RESULTADOS DE APRENDIZAJE (Competencias)

INGENIERÍA EN ELECTRÓNICA INDUSTRIAL

CG10 - Capacidad de trabajar en un entorno multilingüe y multidisciplinar.

CE21 - Conocimiento de los fundamentos y aplicaciones de la electrónica digital y microprocesadores.

CE24 - Capacidad para diseñar sistemas electrónicos analógicos, digitales y de potencia.

PROGRAM

CHAPTER 1. LOGIC SIMPLIFICATION, OPERATIONS AND CODE

1.1 Boolean algebra

1.2 De Morgan’s theorems

1.3 Standard forms of boolean expressions

1.4 The Karnaugh map

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CHAPTER 2. LATCHES, FLIP-FLOPS AND TIMERS

2.1 Introduction to sequential circuits

2.2 Latches

2.2.1 The S-R Latch

2.2.2 The gated S-R Latch

2.2.3 The D Latch

2.3 Edge-triggered Flip-Flops

2.3.1 The S-R Flip-Flop

2.3.2 The D Flip-Flop

2.3.3 The J-K Flip-Flop

2.3.4 The T Flip-Flop

2.4 Monostables (one-shots)

2.5 The 555 timer

CHAPTER 3. SHIFT REGISTERS

3.1 Shift Registers

3.1.1 Serial In / Serial Out

3.1.2 Serial In / Parallel Out

3.1.3 Parallel In / Parallel Out

3.1.4 Parallel In / Serial Out

3.2 Time delay

3.3 Examples of registers:

- 8-bit serial in/parallel out shift register 74HC164
- 4-bit shift register 74195
- 74194 4-bit Bidirectional Serial In /Serial Out Register

CHAPTER 4. COUNTERS

4.1 Concept of counter

4.2 Asynchronous counters

4.3 Synchronous counters

4.4 Other counters: up/down counters, Johnson counter, ring counter

CHAPTER 5. FINITE STATE MACHINES (FSM)

5.1 State Machine Definition

5.2 Main blocks of a state machine

5.3 Finite State Machine models

5.4 Advantages of using state machine design

5.5 FSM general design procedure

CHAPTER 6. SIGNAL INTERFACING AND PROCESSING

6.1 Sampling and anti-aliasing filter

6.2 Analog to digital conversion: holding and quantization, SQNR and errors

6.3 Analog to digital conversion methods:

6.3.1 Flash ADC

6.3.2 SAR ADC

6.3.3 Pipeline ADC

6.3.4 Sigma-delta ADC

6.3.3 Successive approximation ADC

6.4 Digital to analog conversion methods:

6.4.1 Binary-weighted-input DAC

6.4.2 R-2R ladder DAC

EDUCATIONAL ACTIVITIES

4 ECTS: 100-120 working hours, are distributed as follows:

- Theory and exercises sessions: 35 hours
- Lab sessions (computer): 6 hours
- Lab sessions (hands-on): 4 hours
- Projects: 15 hours
- Tutorization: 3 hours
- Personal study: 50 hours
- Evaluation: 4 hours

ASSESSMENT

ORDINARY ASSESSMENT

The final mark will be the sum of the following evaluations:

- Written Exam (**55%**)
- Multisim (**25%**)
- Lab sessions (hands-on) (**10%**)
- Challenge in group:

- Mininum required: Clock design and simulation with Multisim: **10%**
- Extra-points (up to **15%**):
  - Fabrication of the counter: **10%**
  - Challenge of minimum implementation cost: **5%** extra (1st: 5%, 2nd : 2.5%)

Each part requires a minimum mark of 5 over 10 to pass.

EXTRAORDINARY ASSESSMENT

The scores of the parts already passed in the ordinary call willl be kept for the extraordinary call.

The final mark will be the sum of the following evaluations:

- Written Exam (**55%**)
- Multisim (**25%**)
- Lab sessions (hands-on) (**10%**)
- Challenge in group: Clock design and simulation with Multisim: **10%**

Notes:

- The students with special educative needs will contact the Student Coordination Office to obtain the corresponding authorization to their particular cases. This authorization will be sent to the lecturer by the student. It is recommended to do this at the beginning of the semester.
- Any attempt of fraud, copy, plagiarism or other irregular behaviours are a severe infraction of the academic integrity code, as explained in section IV of the document "Normas de disciplina académica de los estudiantes" within the "Sistema de normas sobre la convivencia en la Universidad de Navarra".

OFFICE HOURS

Contact via e-mail to arrange an interview:

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- Javier García: jgmunoz@unav.es

BIBLIOGRAPHY

Basic bibliography

Digital Fundamentals, Floyd, ISBN: 0-13-235923-8 Localízalo en la biblioteca

Digital Logic State Machine Design, Comer, Oxford University Press, ISBN 0-19-510723-3 Localízalo en la biblioteca

Complementary bibliography

Digital Design, Principles and Practices, Fourth Edition, John F. Wakerly, Pearson-Prentice Hall, ISBN 0-13-186389-4 Localízalo en la biblioteca Localízalo en la biblioteca (2a. ed.)

Digital Systems, Principles and Applications, 9th Edition, R.J. Tocci, N.S. Widmer, G.L.Moss, Pearson-Prentice Hall, ISBN 0-13-121931-6 Localízalo en la biblioteca

Digital Design, Fifth Edition, M. Morris Mano, Michael D. Ciletti, Pearson, ISBN-13: 978-0-273-76452 Localízalo en la biblioteca



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